Amendment to the Specification:

Please replace the third full paragraph on page 4 (beginning at line 3̶ 29) of the specification with the following:

In one embodiment of the invention the encoders 10, 10' are terminated simultaneously within three clock cycles, each with its own tail input ~~bit~~ bits $X(t)$, $X'(t)$. Alternatively, the first encoder 10 is first terminated while the second encoder 10' is disabled, followed by the second encoder 10' being terminated while the first encoder 10 is disabled.

Please replace the first full paragraph on page 6 (beginning at line 15) of the specification with the following:

For rate ½ turbo codes, the tail output bits for each of a first n tail input ~~bit~~ bits (also referred to herein as "the beginning tail bit sequence $X(t)$") are XY_0, and the tail output bits for each of a last n tail bit periods (also referred to herein as "the ending tail bit sequence $X'(t)$") are $X'Y_0'$. For rate 1/3 turbo codes, the tail output bits for each of the first n tail input bits are XXY_0, and the tail output bits for each of the last n tail bits are $X'X'Y_0'$. For a rate 1/4 turbo code, the tail output bits for each of the first n tail input bits are XXY_0Y_1 and the tail output bits for each of the last n tail input ~~bits~~ bit periods are $X'X'Y_0'Y_1'$.